REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering this application and for allowing claims 40-52 and indicating that claims 16-18, 29-32, and 35 contain allowable subject matter.

Disposition of Claims

Claims 1-53 are pending in this application. Claims 1, 25, 33, 36-40, and 52-53 are independent. The remaining claims depend, directly or indirectly, from claims 1, 25, 33, and 40.

Rejections under 35 U.S.C. § 102

Claims 1 and 19-20 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,671,863 ("Gauthier"). For the following reasons, this rejection is respectfully traversed.

Embodiments disclosed in this application are directed to a measuring apparatus for estimating jitter of an electronic device. According to one or more embodiments, as a way to estimate jitter of a DUT, the jitter transfer function of a DUT is obtained. It is known to one skilled in the art that the jitter transferring function of a device is defined to be the ratio of the output jitter of the device to the input jitter signal of the device. Thus, it is noted that the jitter transfer function can be obtained only when *the jitter value of the input signal exists as a non-zero value* because the output jitter value is divided by the input jitter value in the definition.

More specifically, in accordance with one embodiment shown in Figure 3, the jitter transfer function measuring apparatus **101** includes the timing jitter estimator **501**, which calculates an output timing jitter sequence indicating the output timing jitter of an output signal

output from the DUT in response to an input signal to the DUT, and the jitter transfer function estimator **103**, which calculates the jitter transfer function of the DUT based on the output timing jitter sequence.

Accordingly, independent claim 1 requires, in part, a timing jitter estimator operable to calculate an output timing jitter sequence of an output signal based on said output signal output from said electronic device. Independent claim 1 further requires, in part, a jitter transfer function estimator operable to calculate a *jitter transfer function* of said electronic device based on said output timing jitter sequence.

Gauthier relates to a method for optimizing loop bandwidth in a phase locked loop. Referring to Figure 3 and the accompanying text of Gauthier, in impedance networks and circuits, power supply noise may be generated by one or more circuit elements, and all other circuit elements may be affected by the power supply noise. Referring to Figure 4, the optimal loop bandwidth to minimize the influence of the power supply noise can be obtained by modeling a power supply waveform having noise **153, 154** to apply to the PLL **20** and measuring jitter in the output signal **160**. The power supply having noise may be applied to any circuit element in the PLL **20** that requires a power supply, for example, the voltage controlled oscillator **308**, and may cause the voltage controlled oscillator **308** to generate jitter in the output clock.

Gauthier suggests simplifying the power supply noise model by means of using digitized power supply signals having noise. However, it is clear to one skilled in the art that the clock inputs to the PLL in the simulation model of Gauthier are assumed to have *no jitter* (*see* clock input **152**) because Gauthier intends to estimate output jitter caused by power supply noise. That is, Gauthier does not intend to obtain the jitter transfer function of the PLL by calculating with input clock jitter and output clock jitter, but simulates how output clock jitter

depends upon power supply noise. It is clear to one of ordinary skill in the art that in the simulation model of Gauthier, the clock input is assumed to have no jitter because only the dependence of output jitter upon power supply noise should be obtained precisely by the simulation model.

Further, it is noted that Figure 5B of Gauthier merely shows in Laplace transform how each element of the PLL **201** functions to convert clock signals. Thus, Figure 5B of Gauthier is irrelevant to the jitter transfer function, which corresponds to the ratio of output jitter to input jitter.

As such, Gauthier does not disclose at least a timing jitter estimator operable to calculate an output timing jitter sequence of an output signal based on said output signal output from said electronic device, and a jitter transfer function estimator operable to calculate a *jitter transfer function* of said electronic device based on said output timing jitter sequence, as required by claim 1.

In view of the above, Gauthier fails to show or suggest all limitations of independent claim 1. Thus, claim 1 is patentable over Gauthier. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Rejections under 35 U.S.C. § 103

Claims 2-3

Claims 2-3 stand rejected under 35 U.S.C. 103(a) as being obvious over Gauthier in view of U.S. Patent No. 6,573,940 ("Yang"). For the following reasons, this rejection is respectfully traversed.

As discussed above, Gauthier fails to show or suggest at least a timing jitter estimator operable to calculate an output timing jitter sequence of an output signal based on said output signal output from said electronic device, and a jitter transfer function estimator operable to calculate a *jitter transfer function* of said electronic device based on said output timing jitter sequence, which is also required by claims 2-3. Further, Yang does not teach that which Gauthier lacks. Specifically, Yang is only relied upon for teaching the instantaneous phase noise estimator and the re-sampler. However, like Gauthier, Yang is silent with respect to at least the timing jitter estimator and the jitter transfer function estimator.

In view of the above, Gauthier and Yang, whether considered separately or in combination, fail to show or suggest all limitations of claims 2 and 3. Thus, claims 2 and 3 are patentable over Gauthier and Yang. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 4-15, 21-24, and 36

Claims 4-15, 21-24, and 36 stand rejected under 35 U.S.C. 103(a) as being obvious over Gauthier in view of U.S. Patent No. 6,782,404 ("Choudhary"). For the reasons set forth below, this rejection is respectfully traversed.

Claims 4-15 and 21-24 depend, either directly or indirectly, from independent claim 1. Independent claim 36 requires, in part, calculating an output timing jitter sequence, which indicates a plurality of output timing jitter of an output signal, based on said output signal output from said electronic device, and calculating a *jitter transfer function* of said electronic device based on said output timing jitter sequence.

As discussed above, Gauthier fails to show or suggest at least calculating an output timing jitter sequence of an output signal based on said output signal output from said

electronic device, and calculating a *jitter transfer function* of said electronic device based on said output timing jitter sequence. Further, Choudhary does not teach that which Gauthier lacks. Specifically, Choudhary is only relied upon for teaching a plurality of input signals having different jitter amounts. However, like Gauthier, Choudhary is silent with respect to at least calculating an output timing jitter sequence of an output signal based on said output signal output from said electronic device, and calculating a *jitter transfer function* of said electronic device based on said output timing jitter sequence.

In view of the above, Gauthier and Choudhary, whether considered separately or in combination, fail to show or suggest all limitations of claims 4-15, 21-24, and 36. Thus, claims 4-15, 21-24, and 36 are patentable over Gauthier and Choudhary. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 25-26, and 37

Claims 25-26 and 37 stand rejected under 35 U.S.C. 103(a) as being obvious over U.S. Patent No. 5,835,501 ("Dalmia") in view of U.S. Patent Application Publication No. 2002/0032832 ("Dykes"). For the reasons set forth below, this rejection is respectfully traversed.

Independent claim 25 requires, in part, a bit error rate estimator operable to estimate the bit error rate of the electronic device based on a gain of a jitter transfer function of the electronic device. Also, independent claim 37 requires, in part, a bit error rate estimation step of estimating the bit error rate of the electronic device based on a gain of jitter transfer function of the electronic device. Claims 25 and 37 suggest estimating a bit error rate of a DUT, based on a jitter transfer function obtained with respect to the DUT.

Dalmia discloses a bit error rate tester (BERT). The BERT of Dalmia merely shows conventional BERTs, which measure a bit error rate by way of comparing measured input data with expected data. Thus, Dalmia fails to teach or suggest estimating a bit error rate based on the jitter transfer function of a DUT. As explained above, the jitter transfer function is defined as the ratio of output jitter to input jitter, and Dalmia is silent as to the ratio of input and output jitter. Therefore, Dalmia does not show at least estimating the bit error rate of the electronic device based on a gain of a *jitter transfer function* of the electronic device, as required by independent claims 25 and 37.

Further, Dykes does not teach that which Dalmia lacks. Specifically, Dykes is only relied upon for teaching measuring the bit error rate based on an electronic device. However, like Dalmia, Dykes is silent with respect to at least estimating the bit error rate of the electronic device based on a gain of a *jitter transfer function* of the electronic device.

In view of the above, Dalmia and Dykes, whether considered separately or in combination, fail to show or suggest all limitations of claims 25 and 37. Thus, claims 25 and 37 are patentable over Dalmia and Dykes. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 27-28, and 38

Claims 27-28 and 38 stand rejected under 35 U.S.C. 103(a) as being obvious over Dalmia in view of U.S. Patent Application Publication No. 2001/0011893 ("Walker"). For the reasons set forth below, this rejection is respectfully traversed.

Independent claim 27 requires, in part, a jitter tolerance estimator operable to estimate said jitter tolerance of said electronic device based on a gain of a jitter transfer function of said electronic device. Also, independent claim 38 requires, in part, a jitter tolerance

estimation step of estimating said jitter tolerance of said electronic device based on a gain of a jitter transfer function of said electronic device. Claims 27 and 38 suggest estimating a jitter tolerance of a DUT, based on a jitter transfer function obtained with respect to the DUT.

As discussed above, Dalmia merely discloses conventional BERTs, which measure a bit error rate by way of comparing measured input data with expected data. Thus, Dalmia fails to teach or suggest estimating the jitter tolerance of the electronic device based on a gain of a *jitter transfer function* of the electronic device.

Further, Walker does not teach that which Gauthier lacks. Specifically, Walker is only relied upon for teaching measuring the jitter tolerance based on an electronic device. However, like Dalmia, Walker is silent with respect to at least estimating the jitter tolerance of the electronic device based on a gain of a *jitter transfer function* of the electronic device.

In view of the above, Dalmia and Walker, whether considered separately or in combination, fail to show or suggest all limitations of claims 27 and 38. Thus, claims 27 and 38 are patentable over Dalmia and Walker. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 33-34 and 39

Claims 33-34 and 39 stand rejected under 35 U.S.C. 103(a) as being obvious over U.S. Patent No. 6,735,259 ("Roberts") in view of U.S. Patent Application Publication No. 2002/0032832 ("Dykes"). For the reasons set forth below, this rejection is respectfully traversed.

Independent claim 33 requires, in part, a timing estimator operable to estimate an input timing sequence of an input signal for testing said electronic device and an output timing sequence of an output signal output from said electronic device in response to said input signal.

Also, independent claim 39 requires, in part, estimating an input timing sequence of an input signal for testing said electronic device and an output timing sequence of an output signal output from said electronic device in response to said input signal. Claims 33 and 39 suggest estimating the bit error rate of an electronic device based on the timing difference between input and out timing sequences.

Roberts relates to an apparatus measuring a bit error rate of an electronic device. However, the timing estimator disclosed in Roberts is merely used for optimizing a threshold level and sampling timings, but does not estimate an input timing sequence and an output timing sequence. Therefore, Roberts fails to teach or suggest at least estimating an input timing sequence of an input signal for testing said electronic device and an output timing sequence of an output signal output from said electronic device in response to said input signal, as required by independent claims 33 and 39.

Further, Dykes does not teach that which Roberts lacks. Specifically, Dykes is only relied upon for teaching measuring the bit error rate based on an electronic device. However, like Roberts, Dykes is silent with respect to at least estimating an input timing sequence of an input signal for testing said electronic device and an output timing sequence of an output signal output from said electronic device in response to said input signal.

In view of the above, Roberts and Dykes, whether considered separately or in combination, fail to show or suggest all limitations of claims 33 and 39. Thus, claims 33 and 39 are patentable over Roberts and Dykes. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 53

Claims 53 stands rejected under 35 U.S.C. 103(a) as being obvious over Gauthier in view of U.S. Patent Application Publication No. 2003/0063701 ("Eubanks"). For the reasons set forth below, this rejection is respectfully traversed.

Independent claim 53 requires, in part, a jitter transfer function measuring apparatus operable to measure a *jitter transfer function* in said electronic device based on said output instantaneous phase noise.

As discussed above, Gauthier fails to show or suggest at least a jitter transfer function measuring apparatus operable to measure a *jitter transfer function* in said electronic device, which is required by claim 53. Further, Eubanks does not teach that which Gauthier lacks. Specifically, Eubanks is only relied upon for teaching estimating an output instantaneous phase noise. However, like Gauthier, Eubanks is silent with respect to at least a jitter transfer function measuring apparatus operable to measure a *jitter transfer function* in said electronic device.

In view of the above, Gauthier and Eubanks, whether considered separately or in combination, fail to show or suggest all limitations of independent claim 53. Thus, claim 53 is patentable over Gauthier and Eubanks. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591, Reference No. 02008/092002.

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Respectfully submitted,

By _____

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Attachments